

Appl. No. 09/884,675
Amdt. dated September 17, 2004
Reply to Office action of June 30, 2004

REMARKS/ARGUMENTS

Receipt of the Office action dated June 30, 2004 is hereby acknowledged. In that action the Examiner: 1) objected to the title; 2) object to claims 11 and 27 for various informalities; 3) rejected claims 1-3, 13-18, 20-21, 23, 25-26, 29-31 and 33-34 as allegedly anticipated by Adler (U.S. Pat. No. 5,634,023); 4) rejected claims 4 and 6 as allegedly obvious over Adler in view of Le (U.S. Pat. No. 6,721,874); 5) rejected claims 7, 9 and 10 as allegedly obvious over Adler in view of Safford (U.S. Pat. No. 6,681,322); 6) rejected claims 5 and 8 as allegedly obvious over Adler in view of Rahman (U.S. Pat. No. 5765,007); and 7) objected to claims 11-12, 19, 22, 24, 27-28 and 32 as dependent upon a rejected based claim, but otherwise allowable if rewritten in independent form.

With this Response, Applicants amend claims 11-12, 19, 22, 27-28 and 32, cancel claims 26, 29-31 and 33-34, and present new claims 35-37. Reconsideration is respectfully requested.

I. AMENDMENTS TO THE SPECIFICATION

As requested in the Office action dated June 30, 2004, Applicants propose a new title.

Applicants amend paragraph [0029] to avoid any interpretation as to what one skilled in the art may have known prior to the benefit of reading the Applicants' disclosure. No new matter is entered.

II. CLAIM OBJECTIONS

In the Office action dated June 30, 2004, the Examiner objected to claims 11 and 27. With this Response, Applicants have amended claims 11 and 27 to address the Examiner's concerns.

III. EFFECTIVELY ALLOWED CLAIMS

In the Office action dated June 30, 2004, the Examiner indicated that claims 11-12, 19, 22, 24, 27-28 and 32 were dependent upon a rejected based claim, but allowable if rewritten in independent form. With this Response, Applicants amend claims 11-12, 19, 22, 27-28 and 32 to be in independent form. Thus, these claims, as well as claim 24 which depends from claim 22, should now be in a condition for allowance.

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IV. CLAIM REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly anticipated by Adler.

Adler is directed to a "**software** mechanism for accurately handling exceptions generated by speculatively scheduled instructions." (Adler Title (emphasis added)). Rather than dealing with hardware based mechanisms for speculative scheduling of instructions, Adler deals with speculative scheduling by a compiler at compile time.

One approach which takes advantage of [unused instruction issue slots of a processor] **involves rescheduling the order of the computer program instructions at compile time.**

(Adler Col. 1, lines 36-38 (emphasis added)).

When the compiler 20 selects an instruction to schedule speculatively... **If the compiler 20** is unable to locate an available bit the instruction is not rescheduled.

(Adler Col. 1, lines 31-39 (emphasis added)).

Adler further discusses exception handling that is built into the application program by the compiler to handle exceptions generated by compiler-based speculative scheduling.

While executing within the CPU 12, **the compiler 20** produces various data structures which contain information that can be used **by an application program to handle exceptions caused by instructions.**

(Adler Col. 4, lines 7-11 (emphasis added)).

In the executable code after this commit point **the compiler 20** inserts instructions to test the semaphore associated with the speculatively scheduled instruction to determine whether an exception occurred during execution of the speculatively scheduled instruction.

(Adler Col. 5, lines 1-5 (emphasis added)).

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Moreover, Adler distinguishes the disclosed system from hardware based speculative execution and exception handling.

On the other hand, if the instruction was speculatively executed **by hardware**, often times the hardware will have circuits which allow the exception to be processed such that the processor can undo errant transactions.

(Adler Col. 2, lines 3-6 (emphasis added)).

Claim 1, by contrast, specifically recites, "A processor, comprising: a first exception handler that receives and handles critical excepted instructions; and a second exception handler that receives and handles non-critical excepted instructions." Applicants respectfully submit that Adler, being directed to compiler based speculative scheduling and exception handling, fails to teach or suggest the claimed hardware based exception handlers.

Based on the foregoing, Applicants respectfully submit that claim 1, and all claims which depend from claim 1 (claims 2-10), should be allowed.

B. Claim 18

Claim 18 stands rejected as allegedly anticipated by Adler.

Adler is directed to a "**software** mechanism for accurately handling exceptions generated by speculatively scheduled instructions." (Adler Title (emphasis added)). Rather than dealing with hardware based mechanisms for speculative scheduling of instructions, Adler deals with speculative scheduling by a compiler at compile time. (Adler Col. 1, lines 36-38; lines 31-39). Adler further discusses exception handling that is built into the application program by the compiler to handle exceptions generated by compiler-based speculative scheduling. (Adler Col. 4, lines 7-11; lines 1-5). Moreover, Adler distinguishes the disclosed system from hardware based speculative execution and exception handling. (Adler Col. 2, lines 3-6).

Claim 18, by contrast, specifically recites, "An exception handler for a processor that resolves excepted instructions, comprising: a speculative exception handler that receives critical excepted instructions and resolves said critical excepted instructions on a speculative basis; and a non-speculative

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exception handler that receives non-critical excepted instructions and resolves said non-critical excepted instructions on a non-speculative basis." Applicants respectfully submit that Adler, being directed to compiler-based speculative scheduling and exception handling, fails to teach or suggest the claimed hardware based exception handlers.

Based on the foregoing, Applicants respectfully submit that claim 18, and all claim 20 which depends from claim 18, should be allowed.

C. Claim 21

Claim 21 stands rejected as allegedly anticipated by Adler.

Adler is directed to a "**software** mechanism for accurately handling exceptions generated by speculatively scheduled instructions." (Adler Title (emphasis added)). Rather than dealing with hardware based mechanisms for speculative scheduling of instructions, Adler deals with speculative scheduling by a compiler at compile time. (Adler Col. 1, lines 36-38; lines 31-39). Adler further discusses exception handling that is built into the application program by the compiler to handle exceptions generated by compiler-based speculative scheduling. (Adler Col. 4, lines 7-11; lines 1-5). Moreover, Adler distinguishes the disclosed system from hardware based speculative execution and exception handling. (Adler Col. 2, lines 3-6).

Claim 21, by contrast, specifically recites, "A processor, comprising: at least one pipeline with a plurality of stages; at least one pipeline with a plurality of stages; an algorithm for detecting non-executable instructions in said at least one pipeline, wherein said algorithm generates a command that identifies the non-executable instruction and identifies a reason that the non-executable instruction will not execute; a speculative exception handler that receives said command for any non-executable instructions that are critical to processor performance; and a non-speculative exception handler that receives said command for any non-executable instructions that are not critical to processor performance." Applicants respectfully submit that Adler, being directed to compiler-based speculative scheduling and exception handling, fails to teach or suggest the claimed hardware based exception handlers.

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Based on the foregoing, Applicants respectfully submit that claim 21, and all claims which depend from claim 21 (claims 23 and 25), should be allowed.

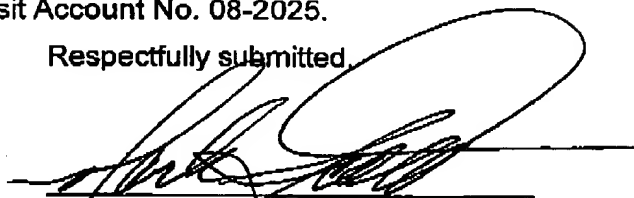
V. CONCLUSION

Applicants respectfully request reconsideration and allowance of the pending claims. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



Mark E. Scott
PTO Reg. No. 43,100
CONLEY ROSE, P.C.
(713) 238-8000 (Phone)
(713) 238-8008 (Fax)
ATTORNEY FOR APPLICANTS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
Legal Dept., M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400